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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/535,233	03/24/2000	Masaya Kadono	SEL 171	1670

7590 08/01/2006

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EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/535,233	KADONO ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☒ Claim(s) *37-42* is/are allowed.

6)☒ Claim(s) *11-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed April 27, 2006 have been fully considered but they are not persuasive.

2. If Applicant Challenges a Factual Assertion as Not Properly Officially Noticed or not Properly Based Upon Common Knowledge, the Examiner Must Support the Finding With Adequate Evidence.

To adequately traverse such a finding, an applicant must specifically point out the supposed errors in the examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art. See 37 CFR 1.111(b). See also Chevenard, 139 F.2d at 713, 60 USPQ at 241 ("[I]n the absence of any demand by appellant for the examiner to produce authority for his statement, we will not consider this contention."). A general allegation that the claims define a patentable invention without any reference to the examiner's assertion of official notice would be inadequate. If applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained. See 37 CFR 1.104(c)(2). See also Zurko, 258 F.3d at 1386, 59 USPQ2d at 1697 ("[T]he Board [or examiner] must point to some concrete evidence in the record in support of these findings" to satisfy the substantial evidence test). If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding. See 37 CFR 1.104(d)(2).

If applicant does not traverse the examiner's assertion of official notice or applicant's traverse is not adequate, the examiner should clearly indicate in the next Office action that the common knowledge or well-known in the art statement is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice or that the traverse was inadequate. If the traverse was inadequate, the examiner should include an explanation as to why it was inadequate.

3. Applicants contend that the prior art rejection is improper because the claimed elements are not shown in Konuma U.S. Patent 6,127,270 herein known as Konuma. Before the element to element matching is address, the Examiner feels that it is important to reveal what both the Application and prior art patent discloses.

The present Application discloses a semiconductor process for forming a semiconductor device such as a thin film transistor (TFT), it not only includes TFT's but also it includes MOS devices, liquid crystal display devices and EC devices (please see page 1 of Applicants disclosure).

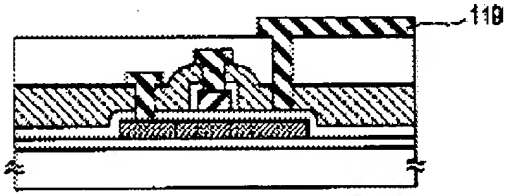
4. Konuma discloses a semiconductor process for applying a solution to a substrate when manufacturing semiconductor devices such as thin film transistors (TFT's), liquid crystal electro-optical devices and the like (column 1, lines 10-15).

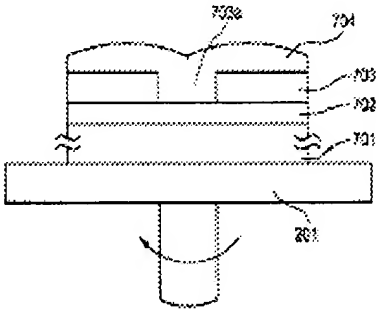
5. The Examiner believes that the difference between the Present Application and the prior art patent of Konuma is the focus of alkaline metals being removed during a semiconductor process. Konuma is silent as to a well known phenomena of alkaline metals (i.e., impurities)

existing on a glass substrate, however, the Examiner provides a supplemental reference since Applicants representative may not be familiar with history of controlling impurities of glass substrates. The first historical reference to discuss is Araujo et al., U.S. Patent 5,578,103 herein known as Araujo. This particular reference is assigned to Corning Incorporated, the maker of the Corning 7059 © glass substrate that is used in the Konuma reference (see column 6, line 64 of Konuma where a Corning #7059 glass substrate is incorporate into a process for fabricating a TFT transistor). Now back to the Araujo reference, this particular reference teaches that a Corning Code 7059 glass (column 5, line 37) contains group II metals also known as alkaline metals (Na, Li^+, K^+, Cs^+, Rb^+, Sr^+, Ba^+, Ca^+, column 2, lines 17-24). In another prior art reference assigned to Semiconductor Energy Laboratory Co., LTD Zhang et al., U.S. Patent 5,529,937, herein known as Zhang teaches that the alkali metal can also come from the silicon film on the substrate, namely the other elements contained in the Si film, for example alkaline elements such as sodium and potassium. The Examiner believes that both references Araujo and Zhang teach that group II metals (alkaline metals) are undesirable and removing them is essential in fabricating improved semiconductor devices. Previously, the Examiner provided a reference to Kern, "Handbook of Semiconductor Cleaning", it is well known that cleaning is a fundamental requirement in today's semiconductor industry. Most wafer fabrication is done in a Clean Room to help eliminate dirt and impurities affecting the semiconductor process. The Examiner request that if cleaning is of relative low importance and not required in Applicant's invention or the prior art, the Applicants should provide an affidavit indicating that cleaning has not been taught prior to Applicants invention. The Examiner would like to note that the Konuma reference teaches a spin etching process and that etching is a form of cleaning.

6. Applicants contend that the Examiner has confused removing unwanted portions of the resist film with removing the patterned resist (see page 2, last paragraph of response to Office Action dated April 27, 2006).

7. With respect to Applicants contention that Konuma fails to teach a patterned resist mask over a semiconductor film to form at lest one semiconductor island and then the patterned resist mask located over said semiconductor island is removed as being not disclosed in Konuma, please note the following. Let's take a look at FIG. F and FIG. 8B below:





8. First and foremost we know that the figure to the left discloses a thin film transistor (TFT) as a final product of a solution applying method as claimed. The semiconductor device contains a substrate **101** (Corning #7059, which has alkali metals which are undesirable as discussed above), next a base film **102** comprising a silicon oxide film is formed above the substrate, next an island like film **103** is formed by patterning the silicon film (see column 7, lines 4-6), next an aluminum film with a thickness of 6000 Å is formed on the silicon film and a photo resist is applied to the upper surface of the aluminum film by spin coating, it is then sub-

sintered at 90 °C, exposed to light, developed, main-sintered, and patterned, thereby forming a hardened photoresist **105**. It is well known to coat a substrate, semi-cure or semi-dry the photoresist before exposing it to light to form a patterned resist film. Next, the substrate is then introduced into a chamber of a spin etching apparatus so that the spin etching forms the gate electrode (because Applicants are aware of the disclosure of this pertinent information, it can be found in column 7, lines 8-14). The Examiner believes that Konuma would suggest forming the silicon island by spin etching because Konuma teaches that is possible to uniformly apply a solution to a substrate on which a resist is formed by ultraviolet light irradiation or ozone water contact to the surface of the resist because, to decrease a contact angel of the solution, in solution applying method in which the moving speed of etching solution over the surface of the substrate is high (column 16, lines 46-52). This would suggest that spin etching can be used not only for the gate electrode but for any film on the substrate as described by Konuma.

9. With respect to cleaning the semiconductor device Konuma teaches that before etching, the substrate may be cleaned by the same manner, (spin etching, see column 7, lines 65-68). It is well known that a buffered hydro-fluoric acid improves the removal of alkali metals as discussed in the "Handbook of Semiconductor Cleaning" by Kern.

10. Applicants contend that Chiyou et al., (JP 11-016866) herein known as Chiyou fails to teach forming island over a said substrate by patterning the crystallized semiconductor film.

11. Please note that Chiyou teaches forming a liquid crystal display. It is well known that liquid crystal display contain transistors comprising the MOS/MIS system. Since the MOS/MIS structure is formed on a planar substrate, the gate electrode of such features normally create the island feature on the surface of the substrate, therefore Applicants argument is moot.

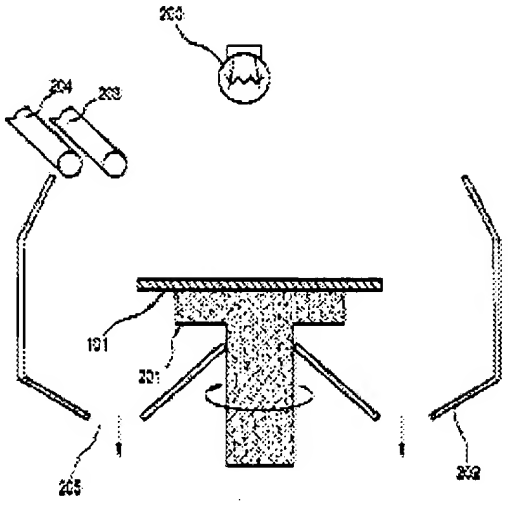
Please note that Applicants do not contend that Konuma fails to teach the claimed subject matter and only that the Examiner did not point out particular well known elements to Applicants representative.

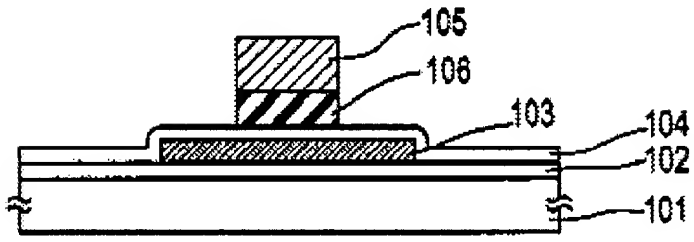
Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 11-18, 23-32 and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Konuma, U.S. Patent 6,127,279.





14. Konuma discloses a semiconductor process as claimed.

Pertaining to claim 11, Konuma teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film **103** over a substrate **101** having an insulating surface **102**;

forming a patterned resist mask over said semiconductor film (not shown, however please note in column 6, lines 62-68, Konuma teaches a fabrication technique of forming a silicon oxide film **103** by sputtering, an amorphous silicon film, i.e., semiconductor film is then formed to a thickness of 500 angstroms, an island like film is only formed after patterning as disclosed in column 7, lines 8-14);

patterning said semiconductor film to form at least one semiconductor island;

spinning the substrate after removing the patterned resist mask (after development of the resist mask, please note that portions of the resist are removed i.e., undeveloped portions); (The Examiner believes that Konuma would suggest forming the silicon island by spin etching because Konuma teaches that is possible to uniformly apply a solution to a substrate on which a resist is formed by ultraviolet light irradiation or ozone water contact to the surface of the resist because, to decrease a contact angel of the solution, in solution applying method in which the moving speed of etching solution over the surface of the substrate is high (column 16, lines 46-52). This would suggest that spin etching can be used not only for the gate electrode but for any film on the substrate as described by Konuma);

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island by the step of applying the etching solution; and then

forming a gate insulating film in contact with said semiconductor film from the surface of which the contaminating impurity has been removed. (With respect to cleaning the semiconductor device Konuma teaches that before etching, the substrate may be cleaned by the same manner, (spin etching, see column 7, lines 65-68). It is well known that a buffered hydro-fluoric acid improves the removal of alkali metals as discussed in the "Handbook of Semiconductor Cleaning" by Kern).

15. Pertaining to claim 12, Konuma teaches a method according to claim 11, wherein the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements (the Examiner takes the position that it is well known to remove contaminants with a fluoric acid solution which was previously discussed by Kern, Also please

see the explanation and the prior art references to the response to arguments above with respect to contaminants of alkali metals with respect to the Corning #7059 substrate used by KONUMA).

16. Pertaining to claim 13, Konuma teaches a method according to claim 11, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg. Ca and Ba .

17. Pertaining to claim 14, Konuma teaches a method according to claim 11, wherein the contaminating impurity is removed by an acidic solution containing fluorine .

18. Pertaining to claim 15, Konuma teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film over a substrate having an insulating surface **702**;

forming a patterned resist mask **703** over said semiconductor film;

patterning said semiconductor film to form at least one semiconductor island;

removing the patterned resist mask located over said semiconductor island;

spinning the substrate after removing the patterned resist mask (this step is done in a cleaning process as described in column 7, lines 67-68);

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island by the step of applying the etching solution;

forming a gate insulating film over said semiconductor island after the contaminating impurities are removed from the surface of the semiconductor island;

spinning the substrate having the gate insulating film;

applying an etching solution to a surface of said gate insulating film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the gate insulating film by the step of applying the etching solution; and then

forming a gate electrode over said gate insulating film after the contaminating impurities are removed from the surface of the gate insulating film (With respect to cleaning the semiconductor device Konuma teaches that before etching, the substrate may be cleaned by the same manner, (spin etching, see column 7, lines 65-68). It is well known that a buffered hydro-fluoric acid improves the removal of alkali metals as discussed in the "Handbook of Semiconductor Cleaning" by Kern.). Please note that Applicants sequence does not provide a new limiting step over what Konuma discloses.

19. Pertaining to claim 16, Konuma teaches a method according to claim 15, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF, hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride (NH_4HF_2) and ammonium fluoride (NH_4F).

20. Pertaining to claim 17, Konuma teaches a method according to claim 15, wherein the contaminating impurity is at least one element selected from periodic table group I elements or periodic table group II elements (please see the rejection of claim 13 above).

21. Pertaining to claim 18, Konuma teaches a method according to claim 15, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba.

22. Pertaining to claims 23 and 27, Konuma teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a gate wiring over a substrate having an insulating surface;

spinning the substrate;

applying an etching solution to surfaces of said substrate and said gate wiring and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the wiring and the insulating surface by the step of applying the etching solution; and then forming a gate insulating film and a semiconductor film over said gate wiring after the contaminating impurities are removed from the surfaces (the Examiner takes the position that since Konuma teaches the fabrication of various semiconductor devices, the wiring layer is inherent).

23. Pertaining to claims 24, 28 and 31, Konuma teaches a method according to claims 11, 23 and 27, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF, hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride (NH_4HF_2) and ammonium fluoride (NH_4F).

24. Pertaining to claim 25 and 29, Konuma teaches a method according to claims 23 and 27, wherein the contaminating impurity is at least one element selected from periodic table group I elements or periodic table group II elements.

25. Pertaining to claims 26 and 30, Konuma teaches a method according to claims 23 and 27, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba..

26. Pertaining to claims 33, 34 and 35, Konuma teaches a method according to claims 15, 23 and 27, wherein the contaminating impurity is removed by an acidic solution containing fluorine (see the rejection of claim 12 above).

27. Claims 19-22 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiyou et al., Patent Abstracts of Japan 11-016866.

28. Chiyou discloses a semiconductor process as claimed.

29. Pertaining to claim 19, Chiyou teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film **3** formed over a substrate **1** having an insulating surface **2**;

crystallizing said semiconductor film [0052];

forming a patterned resist mask over said crystallized semiconductor film (please note that it is well known to pattern transistor with a resist prior to etching as disclosed by Chiyou);

patterning the crystallized semiconductor film to form at least one semiconductor island (transistors on a substrate will inherently form islands) over said substrate;

removing the patterned resist mask located over said semiconductor island (a necessary requirement to make functional devices);

spinning the substrate [0051] after removing the patterned resist mask (unwanted portions of the resist mask are removed);

forming at least one semiconductor island over said substrate by patterning the crystallized semiconductor film [see Drawing 3];

applying an etching solution to a surface of said semiconductor film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island; and then

forming a gate insulating film over said semiconductor island after the contaminating impurities are removed from the surfaces by the step of applying the etching solution; and

forming a gate electrode over said gate insulating film (please note that since Chiyou teaches DRAM, EPROM, MPU and switching transistor and a liquid crystal display the gate electrode and gate insulating layer is well known to be incorporated in the above devices, particularly liquid crystal displays comprise MOS/MIS structures, for Applicants attempt to overcome the present rejection, a sworn affidavit should be submitted to declare otherwise).

30. Pertaining to claim 20, Chiyou teaches a method according to claim 19, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF), hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride (NH_4HF_4) and ammonium fluoride (NH_4F) (LAL500).

31. Pertaining to claim 21, Chiyou teaches a method according to claim 19, wherein the contaminating impurity is at least one element selected from periodic table group I elements or periodic table group II elements (the Examiner takes the position that it is well known that metal ions from the group I and group II elements of the periodic table as conventional contaminants for the silicon process).

32. Pertaining to claim 22, Chiyou teaches a method according to claim 19, wherein the contaminating impurity element is at least one element selected from the group consisting of Na,

K, Mg, Ca and Ba (the examiner takes the position that the claimed elements are one of the major sources of contaminants).

33. Pertaining to claim 36, Chiyou teaches a method according to claim 19, wherein the step of crystallization is performed by irradiating a laser light [0046].

Allowable Subject Matter

34. Claims 37-42 allowed.

35. The following is an examiner's statement of reasons for allowance: the prior art does not anticipate nor render obviousness as to a second spin etching step.

36. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

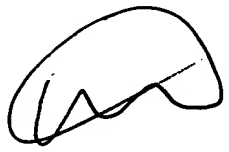
38. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

40. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



W. David Coleman
Primary Examiner
Art Unit 2823

WDC